DATA SHEET

TDA8542
2 × 1 W BTL audio amplifier

Preliminary specification
Supersedes data of 1996 May 06
File under Integrated Circuits, IC01

1997 Feb 19

Philips
Semiconductors

PHILIPS

2 × 1 W BTL audio amplifier TDA8542

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8542(T) is a two channel audio power amplifier for an output power of 2 × 1 W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The TDA8542T comes in a 16 pin SO package and the TDA8542 in a 16 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Motor-driver (servo).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	15	22	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8542T	SO16L	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8541	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

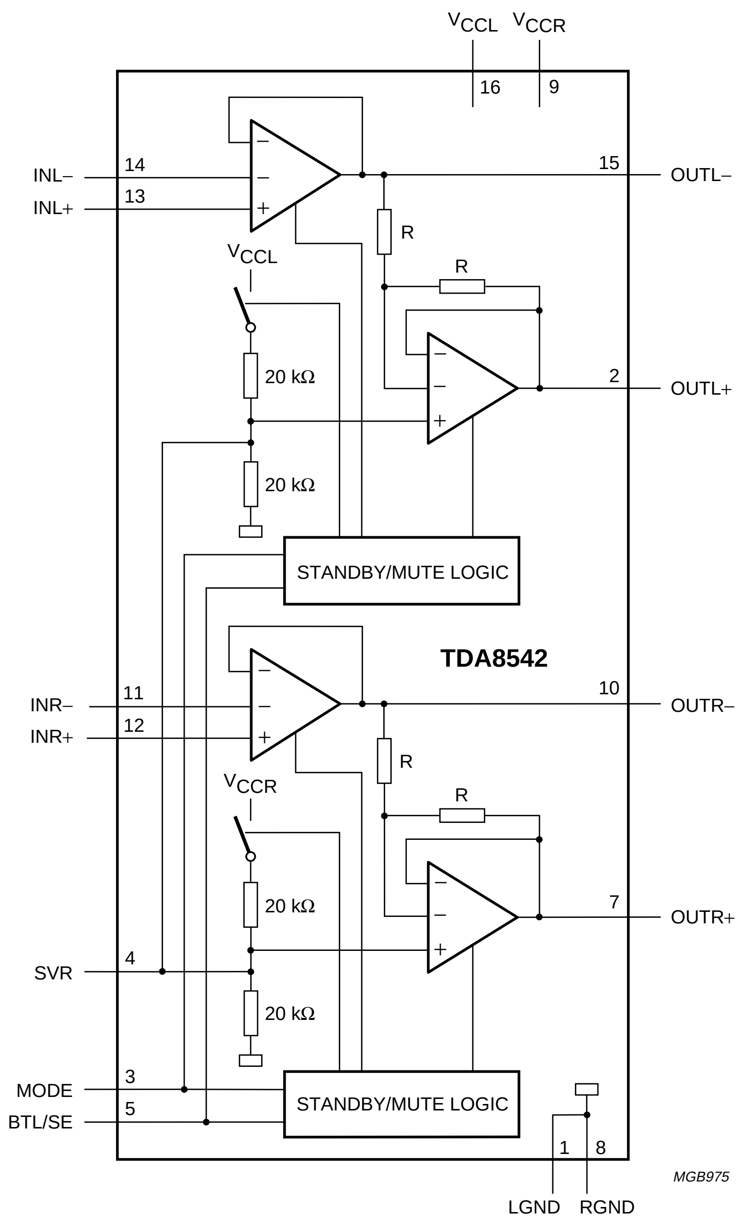


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LGND	1	ground, left channel
OUTL+	2	positive loudspeaker terminal, left channel
MODE	3	operating mode select (standby, mute, operating)
SVR	4	half supply voltage, decoupling ripple rejection
BTL/SE	5	BTL loudspeaker or SE headphone operation
n.c.	6	not connected
OUTR+	7	positive loudspeaker terminal, right channel
RGND	8	ground, right channel
V_{CCR}	9	supply voltage, right channel
OUTR–	10	negative loudspeaker terminal, right channel
INR–	11	negative input, right channel
INR+	12	positive input, right channel
INL+	13	positive input, left channel
INL–	14	negative input, left channel
OUTL–	15	negative loudspeaker terminal, left channel
V_{CCL}	16	supply voltage, left channel

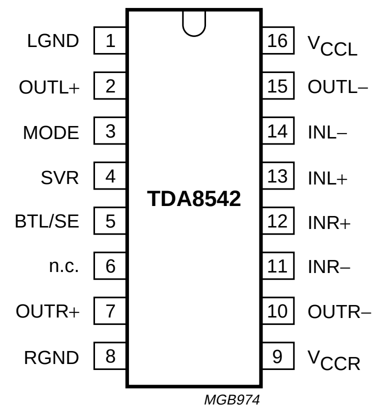


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8542(T) is a 2 × 1 W BTL audio power amplifier capable of delivering 2 × 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage.
The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of a NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

Mode select pin

The device is in the standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} – 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational.
In the range between 1.5 V and V_{CC} – 1.5 V the amplifier

is in mute condition. The mute condition is useful to suppress plop noise at the output caused by charging of the input capacitor.

Headphone connection

A headphone can be connected to the amplifier using two coupling capacitors for each channel. The common GND pin of the headphone is connected to the ground of the amplifier (see Fig.13). In this case the BTL/SE pin must be either on a logic HIGH level or not connected at all.

The two coupling capacitors can be omitted if it is allowed to connect the common GND pin of the headphone jack not to ground, but to a voltage level of $\frac{1}{2}V_{CC}$ (see Fig.13). In this case the BTL/SE pin must be either on a logic LOW level or connected to ground. If the BTL/SE pin is on a LOW level, the power amplifier for the positive loudspeaker terminal is always in mute condition.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–0.3	18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		–	1	A
T_{stg}	storage temperature	non-operating	–55	150	°C
T_{amb}	operating ambient temperature		–40	85	°C
V_{psc}	AC and DC short-circuit safe voltage		–	10	V
P_{tot}	total power dissipation	SO16	–	1.2	W
		DIP16	–	2.2	W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air:		
	TDA8542T (SO16L)	100	K/W
	TDA8542 (DIP16)	55	K/W

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	2.2	5	18	V
I_q	quiescent current	$R_L = \infty$; note 1	–	15	22	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$	–	–	10	μA
V_O	DC output voltage	note 2	–	2.2	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output voltage offset		–	–	50	mV
I_{IN+}, I_{IN-}	input bias current		–	–	500	nA
V_{MODE}	input voltage mode select	operating	0	–	0.5	V
		mute	1.5	–	$V_{CC} - 1.5$	V
		standby	$V_{CC} - 0.5$	–	V_{CC}	V
I_{MODE}	input current mode select	$0 < V_{MODE} < V_{CC}$	–	–	20	μA
V_{BS}	input voltage BTL/SE pin	single ended	0	–	0.6	V
		BTL	2	–	V_{CC}	V
I_{BS}	input current BTL/SE pin	$V_{BS} = 0$	–	–	100	μA

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.
2. The DC output voltage with respect to ground is approximately $0.5 \times V_{CC}$.

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%	1	1.2	–	W
		THD = 0.5%	0.6	0.9	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	0.3	%
G_v	closed loop voltage gain	note 1	6	–	30	dB
Z_i	differential input impedance		–	100	–	kΩ
V_{no}	noise output voltage	note 2	–	–	100	μV
SVRR	supply voltage ripple rejection	note 3	50	–	–	dB
		note 4	40	–	–	dB
V_o	output voltage in mute condition	note 5	–	–	200	μV
α_{cs}	channel separation		40	–	–	dB

Notes

1. Gain of the amplifier is 2 × R2/R1 in test circuit of Fig.3.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_S = 0 Ω at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with a 1 V (RMS) input voltage in a bandwidth of 20 kHz, so including noise.

TEST AND APPLICATION INFORMATION

Test conditions

Because the application can be either Bridge-Tied Load (BTL) or Single-Ended (SE), the curves of each application are shown separately.

The thermal resistance = 55 K/W for the DIP16; the maximum sine wave power dissipation for T_{amb} = 25 °C is:

$$\frac{150-25}{55} = 2.3\ \text{W}$$

For T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150-60}{55} = 1.7\ \text{W}$$

BTL application

T_{amb} = 25°C if not specially mentioned, V_{CC} = 5 V, f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

The BTL application diagram is illustrated in Fig.3.

The quiescent current has been measured without any load impedance. The total harmonic distortion as a function of frequency was measured with a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies, increasing the value of C3 increases the performance of the SVRR. The figure of the mode select voltage (V_{ms}) as a function of the supply voltage shows three areas; operating, mute and standby. It shows, that the DC-switching levels of the mute and standby respectively depends on the supply voltage level.

SE application

T_{amb} = 25°C if not specially mentioned, V_{CC} = 7.5 V, f = 1 kHz, R_L = 4 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

The SE application diagram is illustrated in Fig.14.

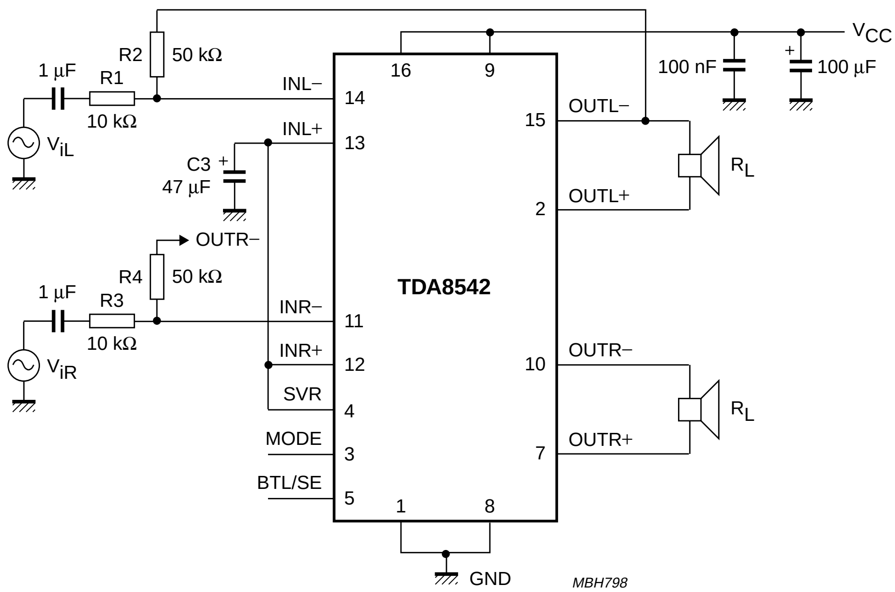
If the BTL/SE pin (pin 5) is connected to ground, the positive outputs (pins 2 and 7) will be in mute condition with a DC level of ½V_{CC}. When a headphone is used (R_L ≥ 25 Ω) the SE headphone application can be used without output coupling capacitors; load between negative output and one of the positive outputs (e.g. pin 2) as common pin.

Increasing the value of electrolytic capacitor C3 will result in a better channel separation. Because the positive output is not designed for high output current (2 × I_o) at low load impedance (≤16 Ω), the SE application with output capacitors connected to ground is advised. The capacitor value of C4/C5 in combination with the load impedance determines the low frequency behaviour. The THD as a function of frequency was measured using a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies, increasing the value of C3 increases the performance of the SVRR.

General remark

The frequency characteristic can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.

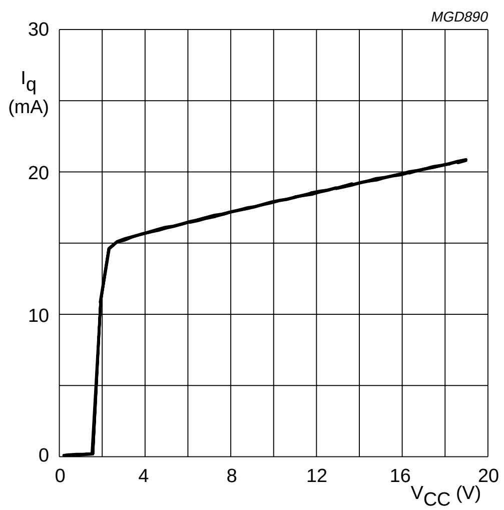
BTL APPLICATION



$$\text{Gain left} = 2 \times \frac{R2}{R1}$$

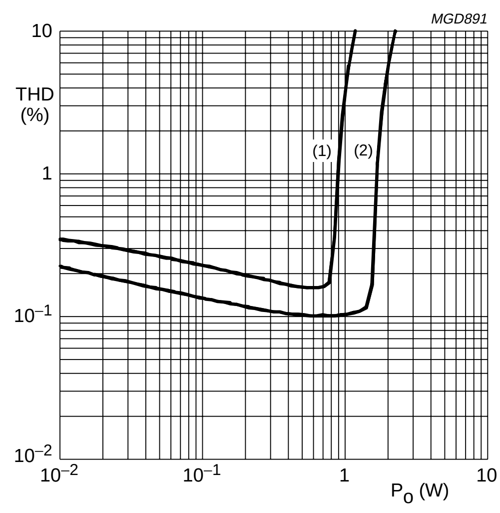
$$\text{Gain right} = 2 \times \frac{R4}{R3}$$

Fig.3 BTL application.



RI = ∞.

Fig.4 I_q as a function of V_{CC}.

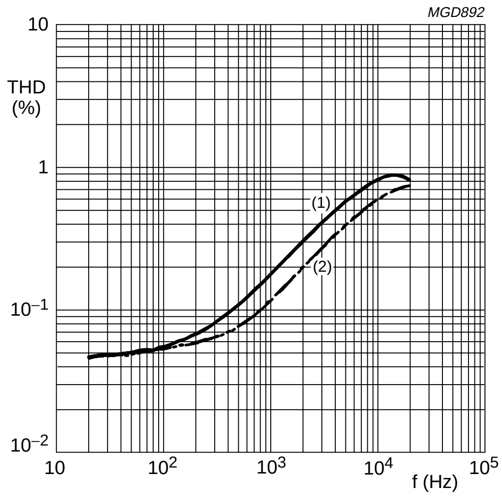


f = 1 kHz, G_v = 20 dB.

(1) V_{CC} = 5 V, R_L = 8 Ω.

(2) V_{CC} = 9 V, R_L = 16 Ω.

Fig.5 TDH as a function of P_o.

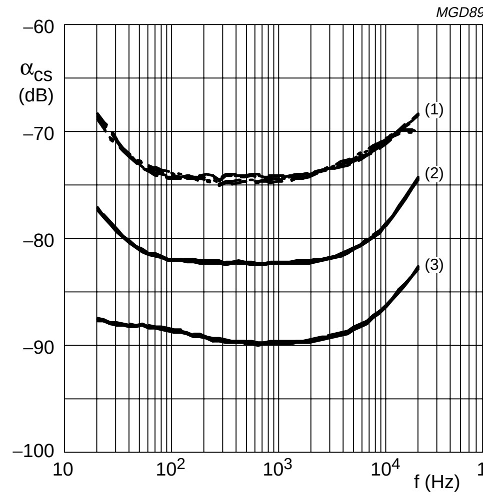


P_o = 0.5 W, G_v = 20 dB.

(1) V_{CC} = 5 V, R_L = 8 Ω.

(2) V_{CC} = 9 V, R_L = 16 Ω.

Fig.6 THD as a function of frequency.



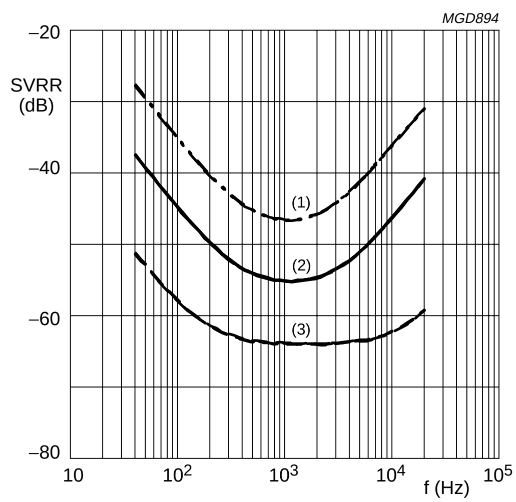
V_{CC} = 5 V, V_o = 2 V, R_L = 8 Ω.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig.7 Channel separation as a function of frequency.



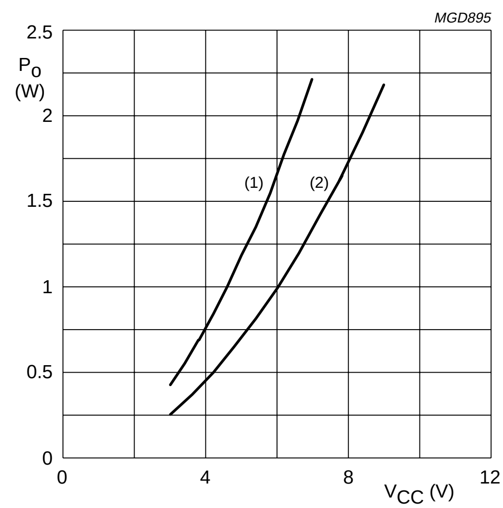
V_{CC} = 5 V, R_s = 0 Ω, V_r 100 mV.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig.8 SVRR as a function of frequency.

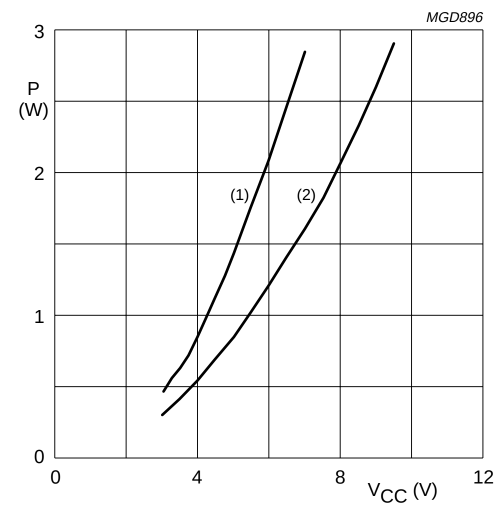


THD = 10%.

(1) V_{CC} = 5 V, R_L = 8 Ω.

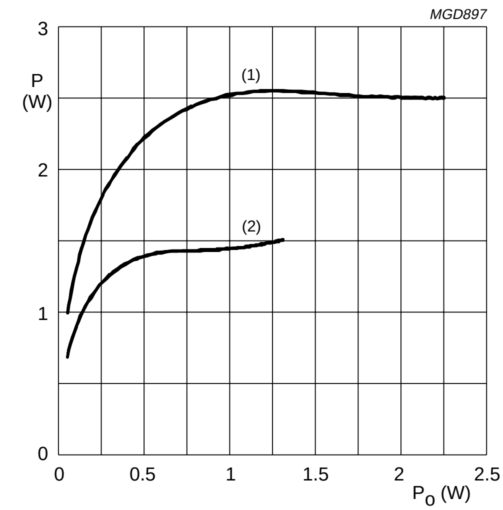
(2) V_{CC} = 9 V, R_L = 16 Ω.

Fig.9 P_o as a function of V_{CC}.



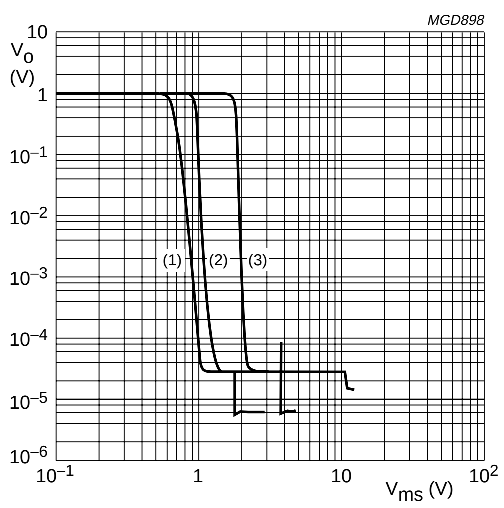
(1) $R_L = 8\ \Omega$.
(2) $R_L = 16\ \Omega$.

Fig.10 Worst case power dissipation as a function of V_{CC}.



Sine wave of 1 kHz.
(1) $V_{CC} = 9$ V, $R_L = 16\ \Omega$.
(2) $V_{CC} = 5$ V, $R_L = 8\ \Omega$.

Fig.11 P_{dis} as a function of P_o.



Band-pass = 22 Hz to 22 kHz.
(1) $V_{CC} = 3$ V.
(2) $V_{CC} = 5$ V.
(3) $V_{CC} = 12$ V.

Fig.12 V_o as a function of V_{ms}.

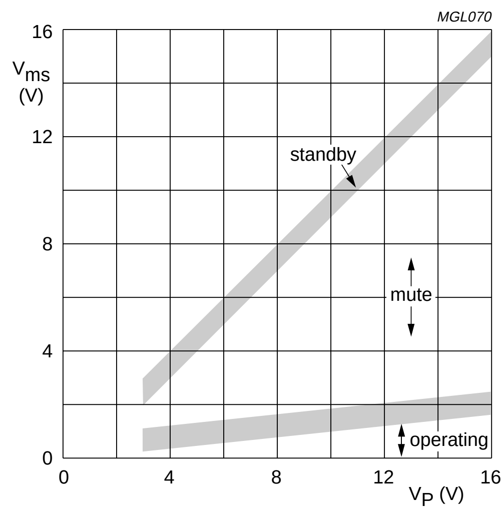


Fig.13 V_{ms} as a function of V_P.

SE APPLICATION

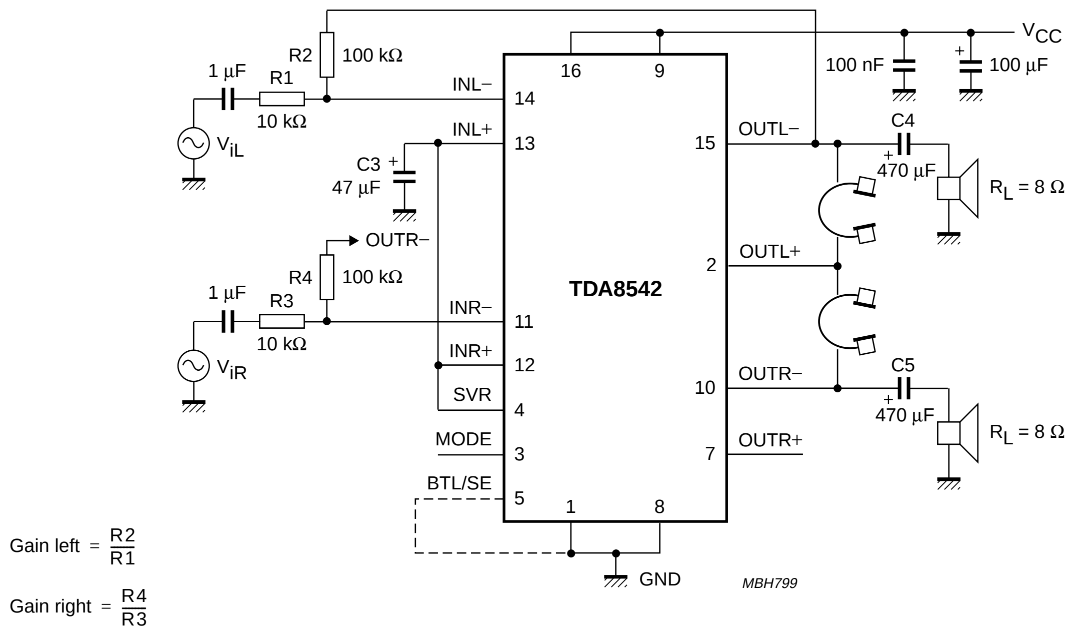
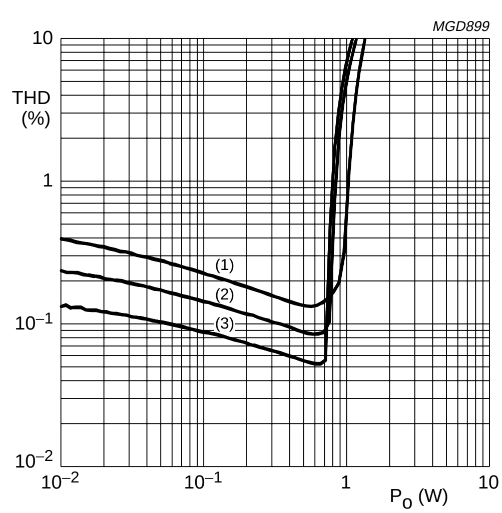
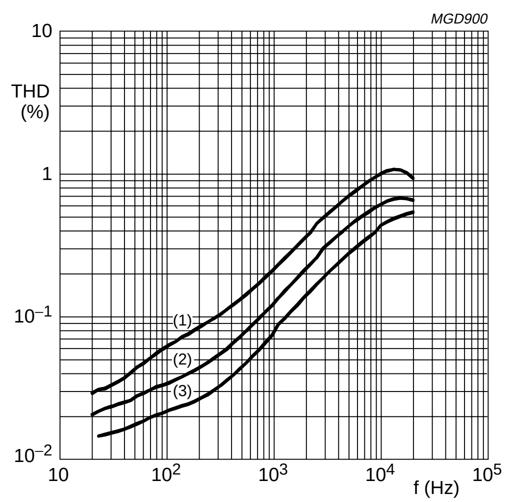


Fig.14 Single-ended application.



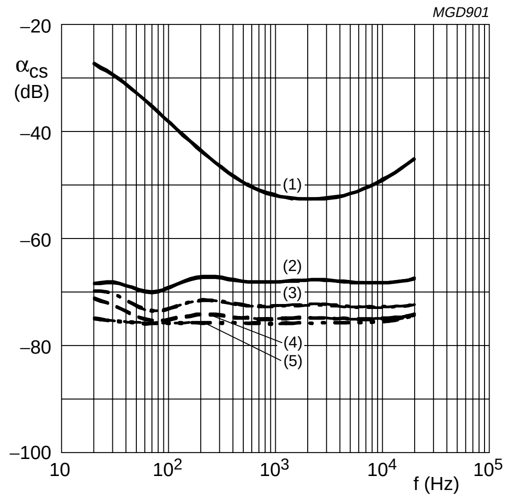
f = 1 kHz, G_v = 20 dB.
(1) V_{CC} = 7.5 V, R_L = 4 Ω.
(2) V_{CC} = 9 V, R_L = 8 Ω.
(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.15 TDH as a function of P_o.



P_o = 0.5 W, G_v = 20 dB.
(1) V_{CC} = 7.5 V, R_L = 4 Ω.
(2) V_{CC} = 9 V, R_L = 8 Ω.
(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.16 THD as a function of frequency.



V_o = 1 V, G_v = 20 dB.

(1) V_{CC} = 5 V, R_L = 32 Ω, to buffer.

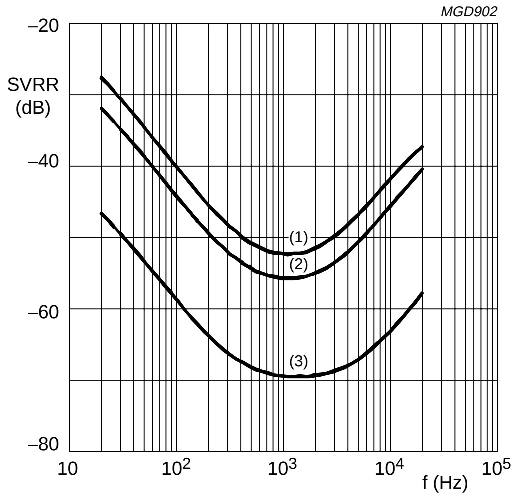
(2) V_{CC} = 7.5 V, R_L = 4 Ω.

(3) V_{CC} = 9 V, R_L = 8 Ω.

(4) V_{CC} = 12 V, R_L = 16 Ω.

(5) V_{CC} = 5 V, R_L = 32 Ω.

Fig.17 Channel separation as a function of frequency.



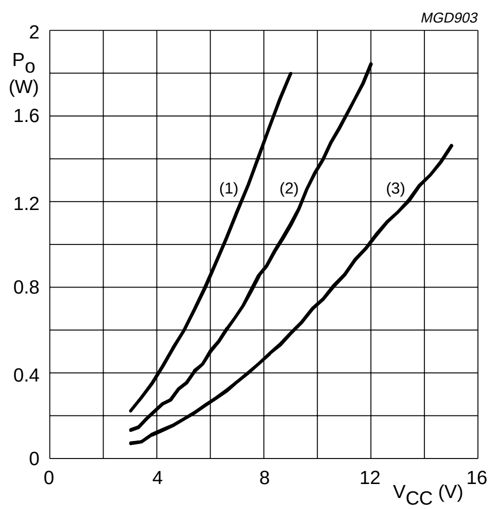
V_{CC} = 7.5 V, R_L = 4 Ω, R_s = 0 Ω, V_r = 100 mV.

(1) G_v = 24 dB.

(2) G_v = 20 dB.

(3) G_v = 0 dB.

Fig.18 SVRR as a function of frequency.



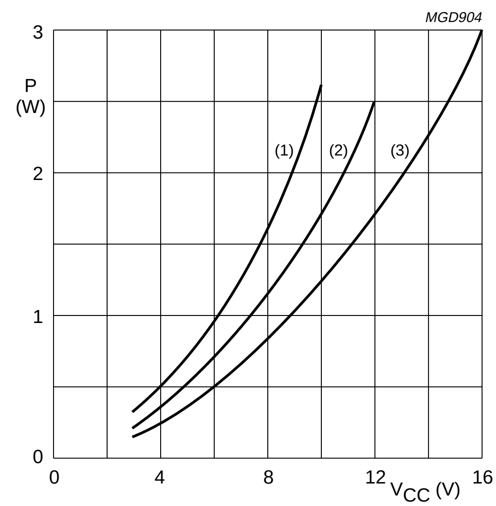
THD = 10%.

(1) R_L = 4 Ω.

(2) R_L = 8 Ω.

(3) R_L = 16 Ω.

Fig.19 P_o as a function of V_{CC}.

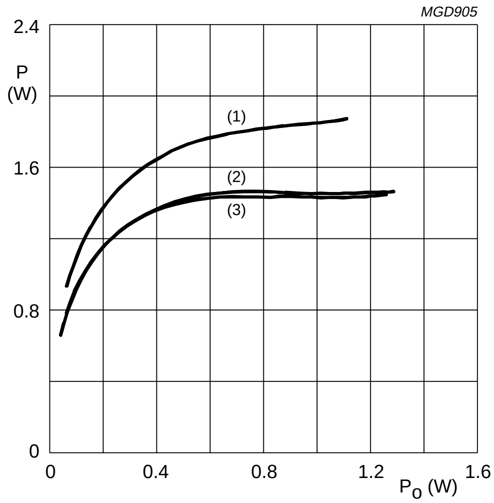


(1) R_L = 4 Ω.

(2) R_L = 8 Ω.

(3) R_L = 16 Ω.

Fig.20 Worst case power dissipation as a function of V_{CC}.



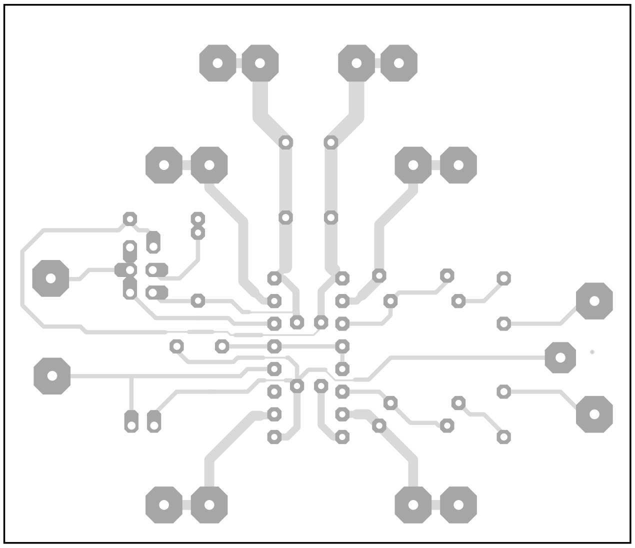
Sine wave of 1 kHz.

(1) V_{CC} = 12 V, R_L = 16 Ω.

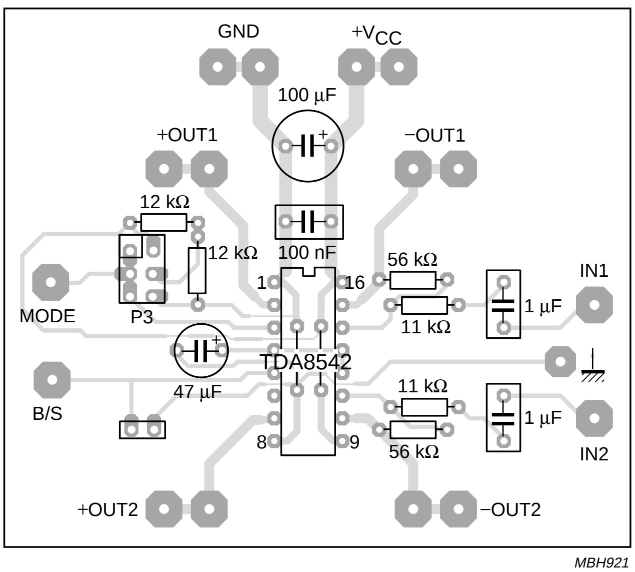
(2) V_{CC} = 7.5 V, R_L = 4 Ω.

(3) V_{CC} = 9 V, R_L = 8 Ω.

Fig.21 P as a function of P_o.



a. Top view.

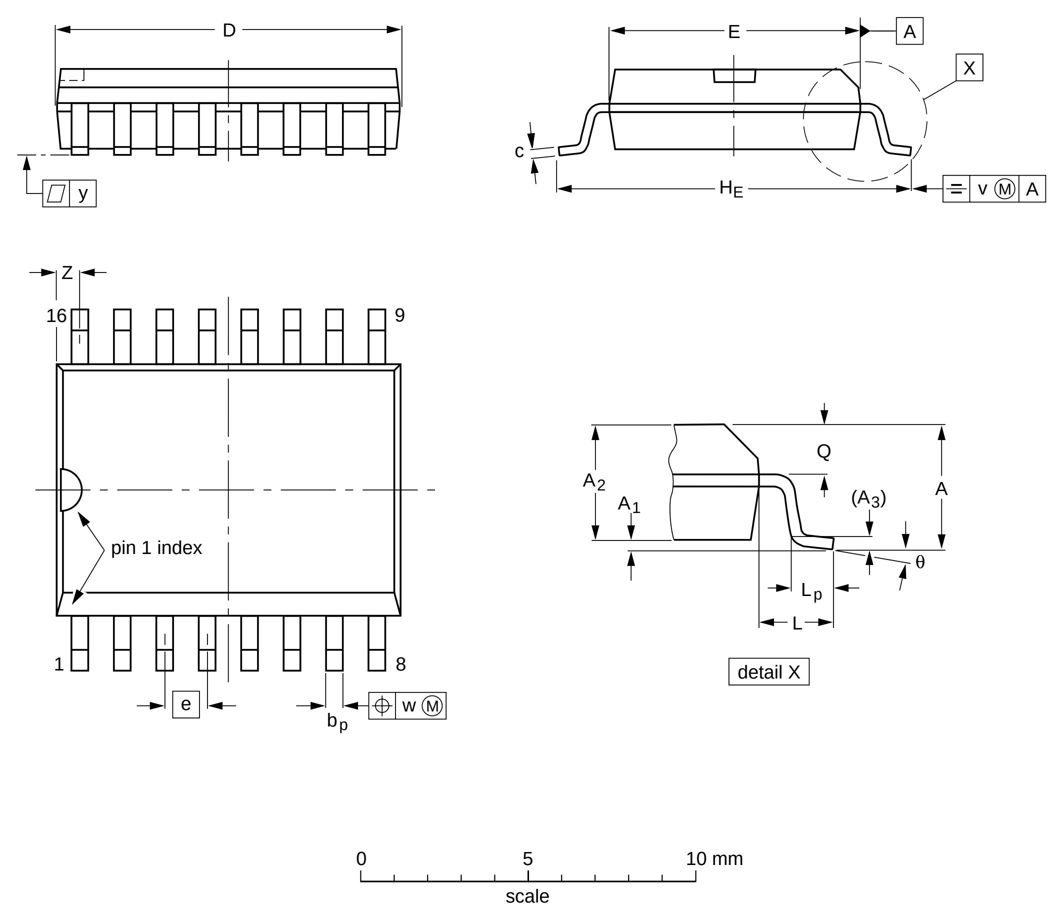


b. Component side.

Fig.22 Printed-circuit board layout (BTL and SE).

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 7.5 mm — SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

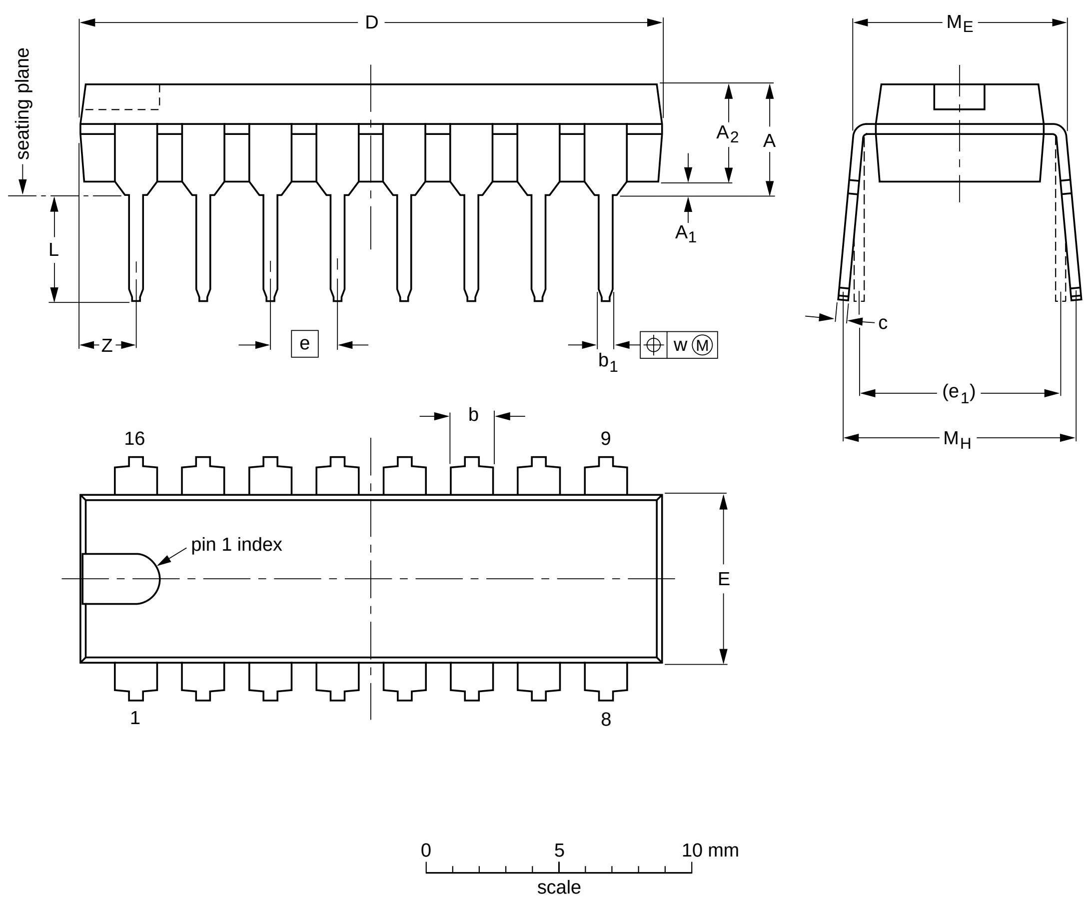
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A1 min.	A2 max.	b	b1	c	D (1)	E (1)	e	e1	L	ME	MH	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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